Andrew Luo

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Objective

Embedded systems and FPGA engineering intern with passion for firmware development, reconfigurable computing, and hardware design. Aspiring to contribute to a free and open-source emerging hardware & software ecosystem. Incoming masters in ECE and seeking research opportunities in hardware design/verification, FPGA engineering, and embedded systems.

Education

Georgia Institute of Technology | Atlanta, GA
Master of Science in Electrical and Computer Engineering — *August 2026 - May 2028*
Bachelor of Science in Computer Engineering, Minor in Physics, GPA 3.7 — *August 2022 - May 2026*

Skills

- **Programming:** C/C++, Python, VHDL, Verilog, Bash, Tcl
- **Platforms:** Linux (Ubuntu, Debian, RHEL, PetaLinux), Windows
- **Hardware:** UltraScale+, RFSOC, Versal, Kria KR260, Altera/Intel FPGA, oscilloscope, logic analyzer
- **Software:** Quartus, Vivado, Git
- **Protocols:** I2C, SPI, UART, JTAG

Experience

Georgia Tech Research Institute | Atlanta, GA — *Fall '24, Summer '25, Aug. '25 – Present*
Full-time Embedded System Hardware/Firmware Co-op @ ELSYS

- Built, designed, and documented two Python-based Qt5 front ends, including a JSON-based config creation/editing tool for validating SOSA conformance (jsonschema).
- Generated multiple customized embedded PetaLinux builds and assisted in writing embedded software in C++ for Kria KR260 MPSoC to enable custom control for a beamforming array.
- Optimized CORDIC unit utilization in PL in I/Q phase and frequency calculations in firmware.
- Created suite of integrated tests in PS-PL on Versal adaptive SoC to ensure SOSA conformance, including I2C and SPI, tested using STM32 H5, ILA, and oscilloscope.
- Designed and implemented finely tunable software defined radio (SDR) with Vita 49.2 packetizer in VHDL on Zynq UltraScale+ RFSOC (PS-PL) for an independent research and development project.

Georgia Institute of Technology | Atlanta, GA — *Jan. '26 – Present*
FPGA Design Verification @ Configurable Computing and Embedded Systems Lab

- Developed formal verification harnesses using CBMC to validate shared memory firmware behavior on the MMU across high-side and low-side processor interfaces, ensuring firmware correctness and memory safety
- Documented verification methods and results to ensure maintainability and reproducibility, advancing the goal of a transparent, open-source voting machine

Georgia Institute of Technology | Atlanta, GA — *Jan. '25 – Present*
Design Verification Team Member @ SiliconJackets

- Implement testbenches in SystemVerilog to verify block-level functional units and pipeline stages of a RV32I CPU with SPI peripheral before eventual tapeout.
- Leverage randomized constrained testing, assertions, and coverage analysis for debugging to achieve 95+% code coverage.
- Develop a working understanding of UVM in aim of creating a standardized and reusable testbench suite.

Leadership

Georgia Institute of Technology | Atlanta, GA — *Aug. '24 – Present*
Peer Leader @ The Hive

- Trained in technical areas (e.g. machine shop, PCB fabrication, waveform generator, oscilloscope, laser cutter).
- Taught end users at The Hive to use and understand equipment; collaborated with a staff network of 150 to ensure safety in the makerspace and foster a community of creativity.

Georgia Institute of Technology | Atlanta, GA — *Aug. '24 – Dec. '24*
ECE Discovery Studio Peer Leader

- Supervised a group of 12 Georgia Tech students three hours a week in the exploration of electrical and computer engineering as a major, technical field of research and a future career.

- Helped students develop the necessary professional communications skillset to articulate their skills, interests, and value through weekly workshops (resume, elevator pitch).

Projects

Embedded Systems Design (ECE 4180) – Skeeball System *Spring '26*

- Engineered a networked Skeeball system utilizing a dual ESP32-C6 architecture and custom 3D-modeled chassis to integrate hardware sensors with real-time game logic.
- Implemented low-latency wireless scoring via ESP-NOW protocol to synchronize event triggers between the sensor node and the primary game controller.
- Developed firmware to interface an e-ink display using SPI, reducing power consumption while maintaining a persistent, high-contrast user interface for score tracking.
- Integrated IR beam break sensors for reliable ball detection, achieving 100% accuracy in score registration through hardware-debounced interrupt routines.